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QUARTERLY TECHNICAL REPORT
1st April 1993 - 30th June 1993

GRANT NUMBER AND TITLE: # N00014-91-J-1441, "DLTS and Dynamic Transconductance Analysis of Deep-Submicron Fully- Depleted SOI MOSFET's".

GRANTEE: George Mason University;Dr.Dimitris E.Ioannou

SCIENTIFIC OFFICER: Dr. Alvin M. Goodman

1.PROGRESS THIS PERIOD

Progress this period was accomplished in two areas, namely hot electron degradation studies of partially- and fully-depleted transistors, and measurement and analysis of relaxation parameters (generation lifetime) in fully-depleted enhancement and accumulation mode transistors.

A summary of the results is given in the attached abstracts: "Successive Charging/Discharging of Gate Oxides in SOI MOSFET's by Sequential Hot Electron Stressing of Front/Back Channel" and "Generation Lifetime Measurements in Fully Depleted Enhancement and Accumulation Mode SOI MOSFET's" submitted for presentation in the forthcoming 1993 IEEE SOI Conference, and "Sequential Stressing of Front/Back Gate Oxides in SOI MOSFET's for Device Characterization and Applications" submitted for presentation in the forthcoming 1993 IEEE IEDM.

A presentation was given at INFOS'93 (8th biennial conference on Insulating Films on Semiconductors) on the topic of "Mechanisms of Hot-Carrier Induced Degradation of SOI (SIMOX) MOSFET's".

A full length paper on the mechanisms of our hot carrier degradation studies is under preparation for IEEE Transactions on Electron Devices.

Two research students are working on the project, Mr. Andrzej Zaleski and Mr. Sinha Shankar.

2.PLANS FOR NEXT PERIOD

(a) Continue the study of hot-carrier degradation mechanisms, and complete a manuscript for submission to IEEE Trans. on Electron Devices.

(b) Study in more detail correlation between impact ionization efficiency and degradation rate during back channel stressing of SOI devices. This can be of importance in case of use of the back interface for erasing purposes in SOI-based flash memories.

(c) Continue the work on accumulation mode, fully depleted devices supplied by IBM and in particular to develop Dynamic Transconductance technique for accumulation mode SOI MOSFET's, and investigate hot-carrier effects in these devices, as compared to enhancement mode MOSFET's.

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(d) Compare the Dynamic Transconductance with Charge Pumping and Subthreshold Slope techniques in an attempt to resolve some apparent discrepancies.

(e) Model the degradation of the static transconductance in SOI MOSFET's with emphasis on high transverse field mobility behavior.

3.POTENTIAL PROBLEM AREAS

(a) Technical:None
(b) Funding:None

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GENERATION LIFETIME MEASUREMENTS IN FULLY DEPLETED ENHANCEMENT AND ACCUMULATION MODE SOI MOSFETS

S. P. Sinha, A. Zaleski, D. E. Ioannou, F. Brady(1)
Department of Electrical and Computer Engineering
George Mason University, Fairfax, VA 22030
(1) IBM Federal Systems Company, Manassas, VA 22110

Several techniques to measure the generation lifetime in SOI MOSFET's have been reported recently, based on the dual-gate Zerbst-type analysis[1]. For partially depleted devices the required deep depletion condition is easily achieved and the measurement is fairly straightforward[2]. For fully depleted devices, however, a more elaborate approach is required to obtain the required generation volume. A method was reported recently for enhancement mode fully depleted transistors[3], where the transients were analysed by using the temporal carrier distributions. The application of this technique, however, requires complicated measurements and data analysis. To our knowledge, no analysis has been reported for accumulation mode devices.

In this work we present a unified analysis for both enhancement and accumulation mode devices, by considering the temporal variation of the quasi-Fermi levels. This leads to an accurate determination of the generation volume, and to the following Zerbst-type expressions for the drain current transients for enhancement eqn.(1) and accumulation eqn. (2) mode devices, respectively:

$$\frac{(C_{oxb}+C_{si})}{2qn_iC_{si}^2}\frac{d}{dt}(KI_d+(V_{gf}-2\phi_f)C_{oxf})^2=\frac{t_{si}K}{\tau_gC_{si}}(I_{d\infty}-I_d) \tag{1}$$

$$\frac{(C_{oxb}+C_{si})}{2qn_iC_{si}^2}\frac{d}{dt}(KI_d+V_{gf}C_{oxf})^2=\frac{t_{si}K}{\tau_gC_{si}}(I_{d\infty}-I_d) \tag{2}$$

where $K=\frac{L}{\mu ZV_d}$ and the symbols have their usual meaning.

In accordance with the Zerbst methodology plotting the left-hand side (LHS) of the above equations as a function of $I_{d\infty}-I_d$ results in a straight line, the slope of which gives τ_g, the generation lifetime. Fig. 1 shows the drain current transient for an enhancement mode device obtained by stepping the back gate voltage from -6V to -20V, while keeping the front gate voltage at 2V and the drain voltage at

.05V. The inset shows the corresponding Zerbst-type straight line fit according to eqn.(1), from the slope of which the lifetime is found to be $\tau_g = .7\mu s$. Fig. 2 shows the corresponding drain current transient for an accumulation mode device obtained from PISCES simulations assuming a lifetime of $\tau_g = .1\mu s$. The value obtained from the Zerbst-type straight line plot (inset) is $\tau_g = .09\mu s$, which is clearly in very good agreement with the assumed value.

The work at George Mason University is supported by DNA through ONR Grant # N00014-91-J-1441.

[1] P.W.Barth, J.B.Angell, IEEE Trans. Electron Devices, vol. ED-27, pp.2252-2255, Dec. 1980.

[2] D.E.Ioannou, S.Cristoloveanu, M.Mukherjee, B.Mazhari, IEEE Electron Device Lett., vol. 11, pp.409-411, Sep. 1990.

[3] N.Yasuda, K.Taniguchi, C.Hamaguchi, Y.Yamaguchi, T.Nishimura, IEEE Trans. Electron Devices, vol.39, pp.1197-1201, May 1992.

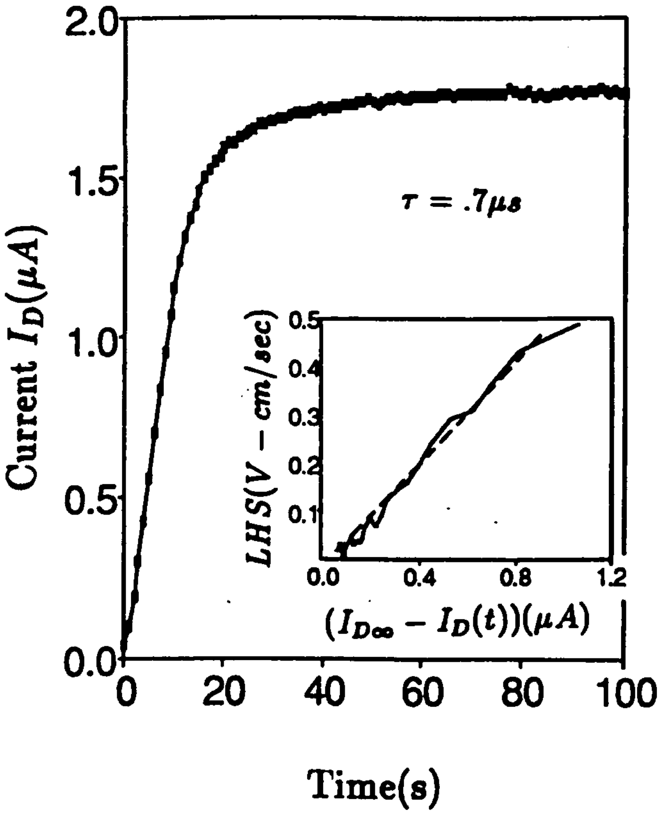

Fig. 1. Typical current transient and (inset) numerical analysis according to (1) for an enhancement mode device.

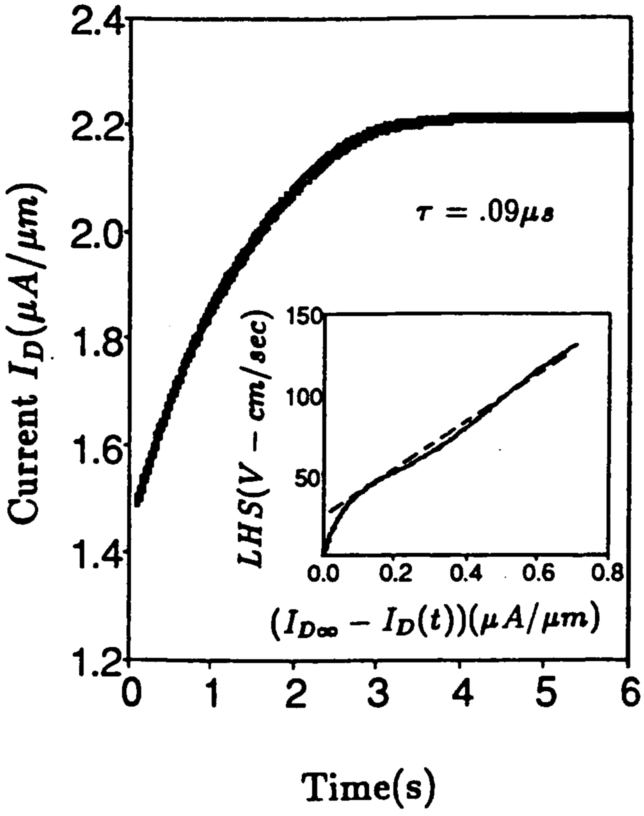

Fig. 2. Simulated (PISCES) current transient and (inset) numerical analysis according to (2) for an accumulation mode device

SUCCESSIVE CHARGING/DISCHARGING OF GATE OXIDES IN SOI MOSFET's BY SEQUENTIAL HOT ELECTRON STRESSING OF FRONT/BACK CHANNEL

Andrzej Zaleski, Dimitris E. Ioannou, George J. Campisi(1), and Harold L. Hughes(1)
Department of Electrical and Computer Engineering
George Mason University, Fairfax, VA 22030
(1) Naval Research Laboratory, Washington, D.C. 20375

As progress is being continuously made on various SOI technologies, there is an increasing need to address the reliability of MOSFET devices and circuits made by these technologies. With ever decreasing device dimensions, degradation caused by hot carriers is especially important. The ability to bias the front and the back gate independently, and the interaction of these two gates, makes the study of hot carrier degradation very challenging, and at the same time provides new opportunities. This interaction may for example result in degradation of a channel during hot carrier stressing of the opposite channel. However, opinion varies as to whether the opposite interface sustains actual damage, or it appears to be degraded through electrostatic coupling. The purpose of this work is to demonstrate that stressing one channel can in fact inject charges into the other channel, and discuss two important applications of this phenomenon: namely, that it can be used as a new tool for the study of the mechanisms of degradation, and for designing erasing schemes for SOI based flash memories. Our measurements were performed on partially and fully depleted SIMOX MOSFET's with LDD and channel lengths down to 0.6 μm.

Figures 1 and 2 show results obtained for a 0.8 μm channel length PD device, which was sequentially stressed for two hours under front channel hot-electron injection conditions (FEI), followed by two hours of back channel hot-electron injection conditions (BEI), and repeating the cycle for a total of thirty six hours. The full recovery of the front channel static characteristics rules out interface state generation during FEI and is caused by hole trapping during the BEI stress. This hole injection into the front gate oxide during back channel stressing is also responsible for the recovery of the front gate threshold voltage to its prestress value. From these and other experimental results as well as PISCES simulations it is concluded that the main cause of degradation is oxide charges trapped by intrinsic and/or induced oxide traps, and that the degradation is a two step process, of trap generation and trap filling. However, under low front gate voltage stress conditions, significant interface state generation also occurs.

Finally, the ability to inject hot-holes and discharge the opposite gate oxide may be explored for possible use in designing SOI flash memory cells with back-channel-based erasing schemes.

The work at George Mason University is supported by DNA through ONR Grant # N00014-91-J-1441.

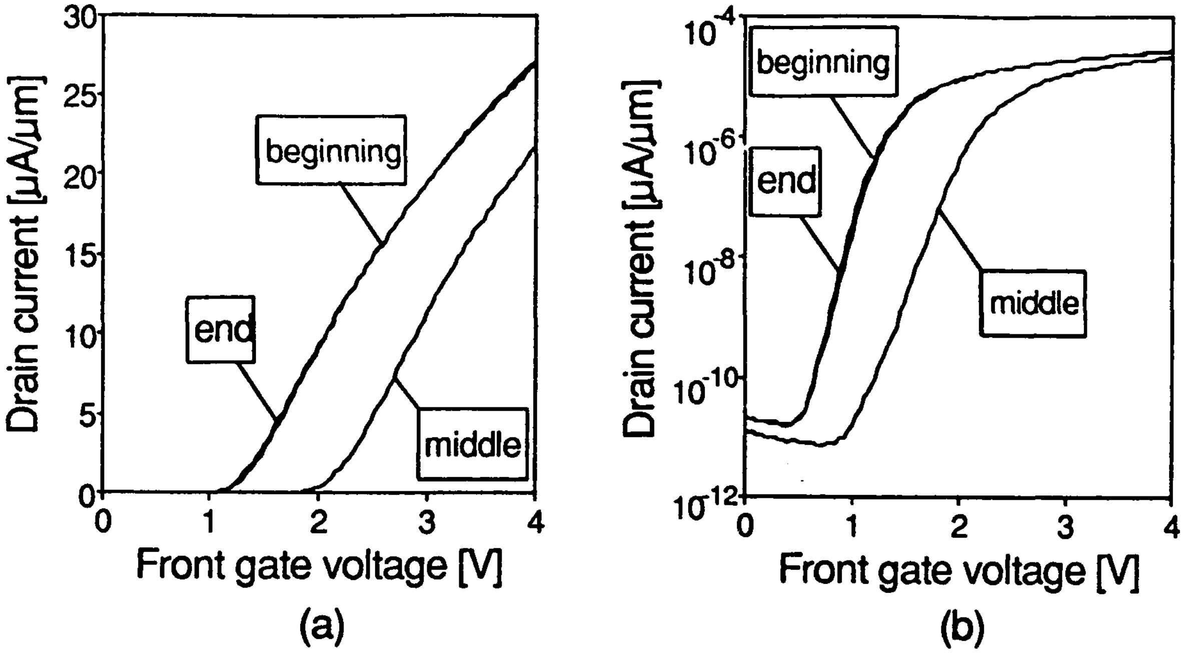

Fig.1: Static (a) I_D vs. V_{G1} and (b) I_D vs. V_{G1} characteristics of a 0.8 μm channel length PD transistor, at the beginning, middle, and the end of the third stress cycle, following hot-electron stressing of the back, front and back channel, respectively. V_D=0.1 V, and V_{G2}=-20 V.

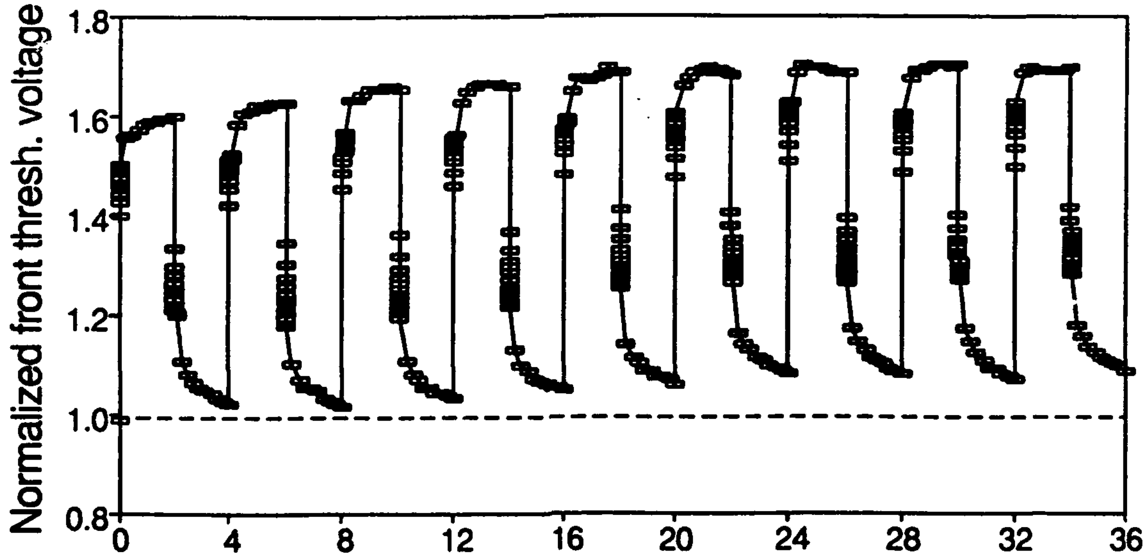

Fig.2: Front threshold voltage, normalized to its prestress values, throughout the duration of stress (nine stress cycles) for the same device as in Fig.1.

Sequential Stressing of Front/Back Gate Oxides in SOI MOSFET's for Device Characterization and Applications

Student Paper - CMOS Devices and Reliability

Andrzej Zaleski, Dimitris E. Ioannou, George J. Campisi(1), and Harold L. Hughes(1)
Department of Electrical and Computer Engineering
George Mason University, Fairfax, VA 22030, tel. (703)993-1583
(1) Naval Research Laboratory, Washington, D.C. 20375

Work at GMU is supported by DNA through ONR Grant # N00014-91-J-1441.

As progress is being continuously made on various SOI technologies, there is an increasing need to address the reliability of MOSFET devices and circuits made by these technologies. With ever decreasing device dimensions, degradation caused by hot-carriers is especially important [1]. The ability to bias the front and the back gate independently and the interaction of these two gates makes the study of hot-carrier degradation in SOI MOSFET's very challenging, and at the same time provides new opportunities. For example this interaction may result in degradation of a channel during hot-carrier stressing of the opposite channel. However, opinion varies as to whether the opposite interface sustains actual damage, or does it appear to degrade through electrostatic coupling. The purpose of this work is to demonstrate that stressing one interface can inject charges into the opposite interface, and to discuss two important applications of this phenomenon: namely, that it can be used as a new tool for studying of the mechanisms of degradation, and it can be applied to the design of novel erasing schemes for SOI-based flash memories. Our experiments were performed on partially and fully depleted SIMOX MOSFET's with LDD's and channel lengths down to 0.6 μm.

Figure 1 demonstrates how the sequential stressing of front/back gate oxide influences the front/back threshold voltages $V_{T1,2}$ [2]. Sequentially applied front high V_{G1} electron injection (FEI) and back electron injection (BEI) conditions cause V_{T1} and V_{T2} to increase and decrease accordingly. For the sample in Fig.1, V_{T1} increased during FEI (period I) recovers completely during following BEI (II). Similarly, the V_{T2} degraded during BEI (II) shows partial recovery during the subsequent FEI (III). Stress conditions suggest that the reason for the observed threshold voltages recovery is hot-holes created by impact ionization at one interface and injected into the gate oxide of the opposite interface, accumulated during stress. To eliminate other possible mechanisms of electron detrapping (i.e. F-N detrapping across the gate-to-drain overlap region [3]), an additional "cross-check" is performed by making the experiments described in Fig.2. It is clear in Fig.2 that a significant $V_{T1,2}$ recovery requires the actual opening of the opposite channel which confirms that the recovery is by hot-holes created at the opposite interface. Figure 3 and 4 show examples of the extent of the transistor parameters recovery for different technologies. From Fig.3 we conclude that the electron trapping dominates other degradation mechanisms during front channel stressing, especially at high V_{G1}. The ability to overshoot the V_{T1} recovery for two other technologies (Fig.4) indicates that a very efficient hot-holes injection can be obtained using the described procedure. In Fig.5, D_{it} for the front interface increases after low V_{G1} front channel stressing (FHI). This is consistent with the results in Fig.3. for which a part of the damage was not recoverable after the low V_{G1} stressing. Finally, in Fig.6 we determine the trapping time constants that are observed in Fig.1a. Changes of V_{T1} during period I (FEI) can be best fit [4] with one time constant, whereas for period III (next FEI) a second time constant has to be added, suggesting two processes involved in the electron trapping. The identical situation occurs at the back interface. From these and other experimental results as well as PISCES simulations it is concluded that the main cause of degradation is oxide charges trapped by intrinsic and/or induced oxide traps, and that the degradation is a two step process, of trap generation and trap filling. On the other hand, under low V_{G1} stress conditions, significant interface state generation also occurs.

The ability to inject hot-holes and discharge the opposite gate oxide may be explored for possible use in designing SOI flash memory cells [5] with back-channel-based erasing schemes. This approach may offer several advantages, but also poses some challenges due to the relatively high voltages region and significant oxide charge trapping involved in the use of the buried interface for the erasing purpose. These issues will be addressed in our presentation.

References:

[1] C.Hu et al, IEEE Trans. Elec. Dev., ED-32(2), p.375, 1985.
[2] A.Zaleski et al, IEEE Elec. Dev. Lett., to be published in Sep. 1993.
[3] B.S.Doyle et al, IEEE Trans. Elec. Dev., 40(5), p.980, 1993.
[4] B.S.Doyle et al, IEEE Trans. Elec. Dev., 37(8), p.1869, 1990.
[5] K.Yoshikawa et al, IEDM Tech. Dig., p.595, 1992.

	FEI	BEI	FEI	BEI	FEI
Vd [V]	8	7.5	8	7.5	8
Vg1 [V]	8	-2	8	-2	8
Vg2 [V]	-20	75	-20	75	-20

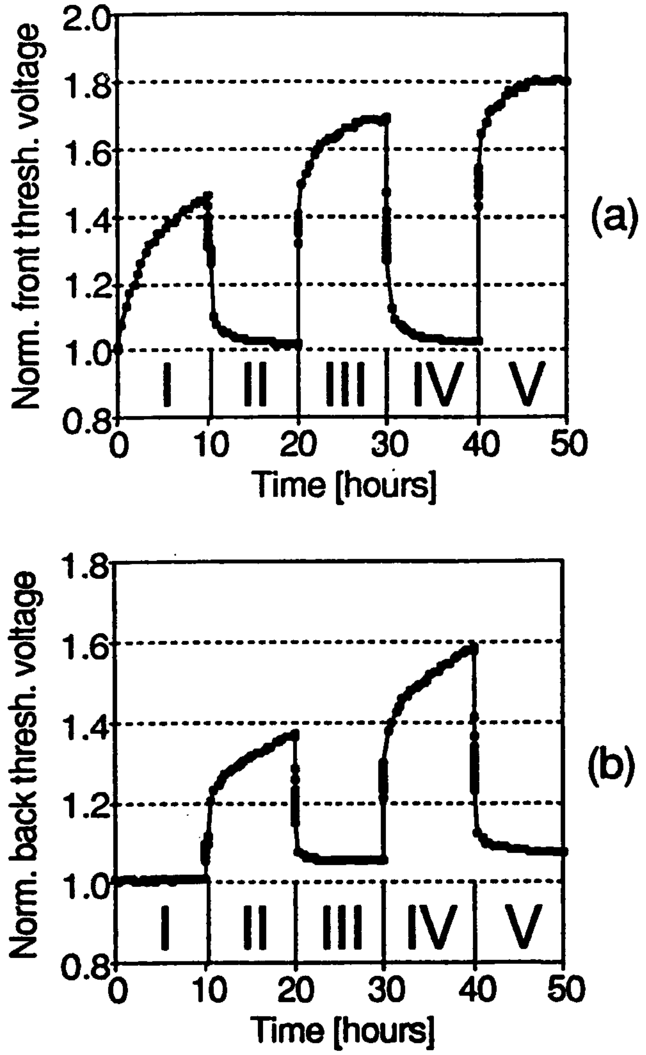

Fig.1. Demonstration of the sequential stressing effect: front (a) and back (b) channel normalized threshold voltage changes during sequential front/back channel hot-electron stressing (I, III, V - FEI, II, IV - BEI; values are at the top of the figure).

	BEI	0's	ACC 1	FEI	0's	ACC 2	BEI
Vd [V]	7.5	0	8	8	0	7.5	7.5
Vg1 [V]	-2	0	-2	8	0	-2	-2
Vg2 [V]	75	0	-20	-20	0	-20	75

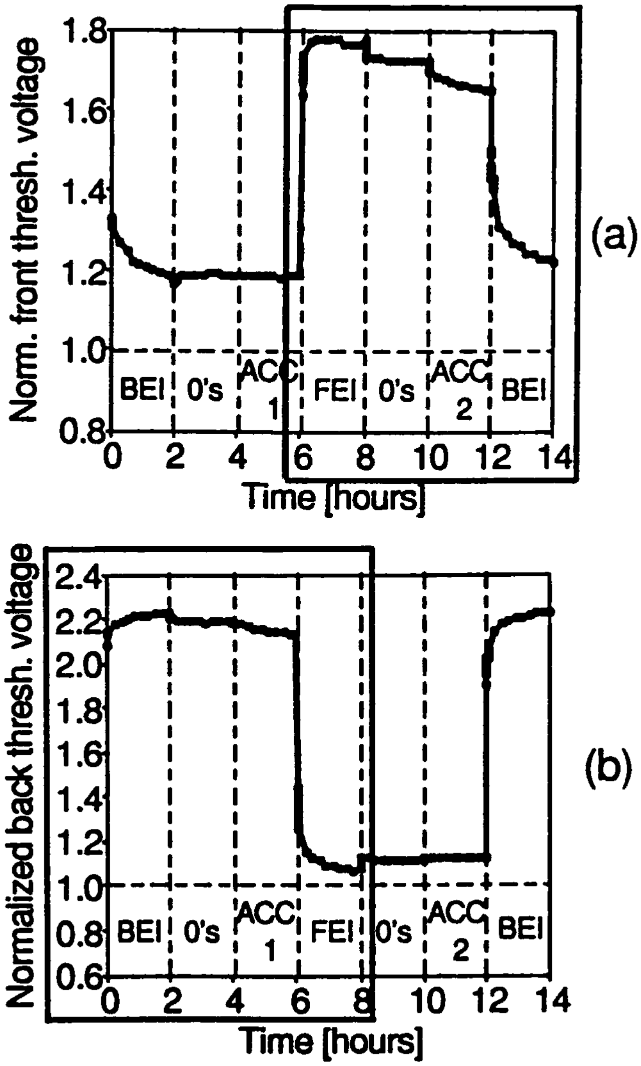

Fig.2. Check-up stressing sequence for the front (a) and back interface (b), to pinpoint the reason of the $V_{T1,2}$ recovery in Fig.1. The applied voltages are at the top of the figure. Comparison of the $V_{T1,2}$ changes during stresses ACC 2 and BEI for the front (a), and ACC 1 and FEI for the back (b) clearly identify opening of the opposite channel as a condition for the significant threshold voltage recovery.

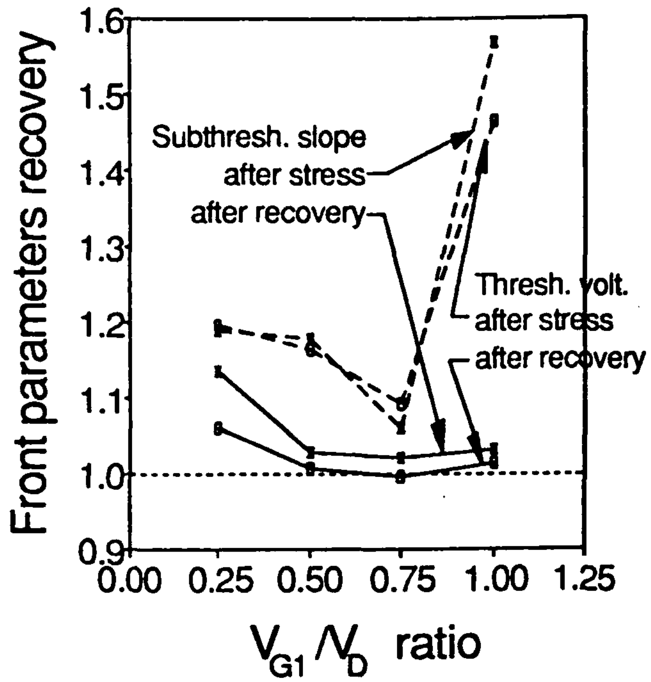

Fig.3. Front threshold voltage and subthreshold slope changes following front channel stress and subsequent BEI as a function of V_{G1}/V_D ratio during the front channel stress. For high V_{G1} both V_{T1} and subthreshold slope recover almost completely but only partial recovery is observed for low V_{G1} stress.

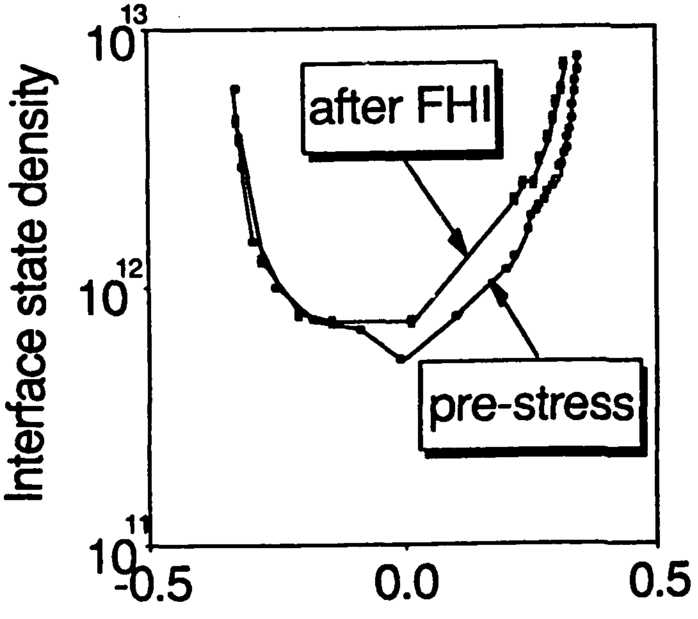

Fig.5. Typical front interface state density D_{it} vs. energy profile before and after front low V_{G1} hole-injection stress (FHI).

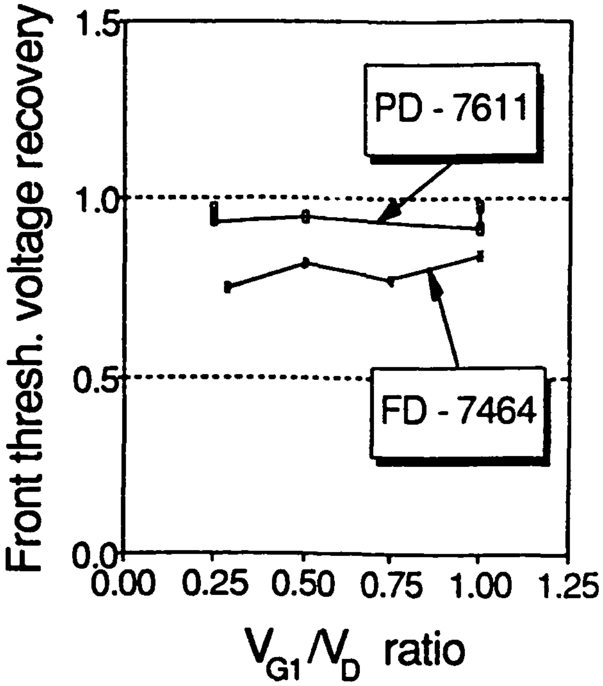

Fig.4. Front threshold voltage recovery of two technologies for which V_{T1} overshoots below its pre-stress value after BEI following front channel stress, as a function of V_{G1}/V_D ratio during the front channel stress.

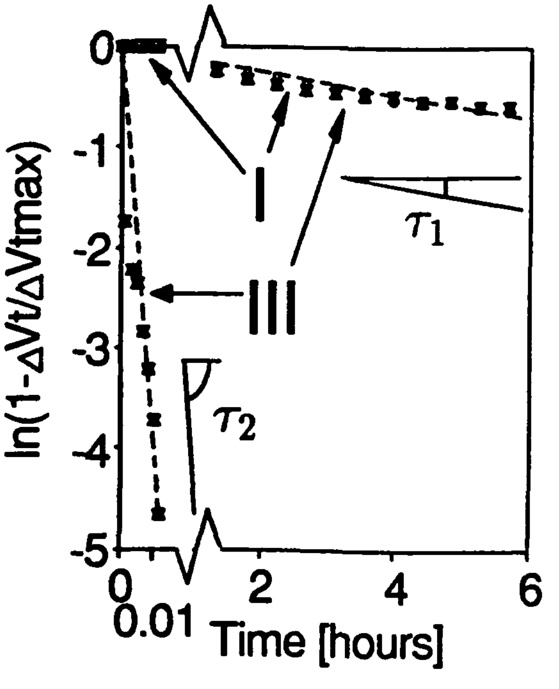

Fig.6. Analysis of data from Fig.1a (periods I and III). Best fit is obtained for period I with one time constant τ_1. For period III two different time constants are required $\tau_{1,2}$. We link these both time constants with oxide trap creation τ_1, and oxide trap filling τ_2 processes. As it can be seen oxide trap creation constants τ_1 overlap for stresses I and III.